

Error tracing in linear and concatenated quantum circuits

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Abstract

Descriptions of quantum algorithms, communication etc. protocols assume the existence of closed quantum system. However, real life quantum systems are open and are highly sensitive to errors. Hence error correction is of utmost importance if quantum computation is to be carried out in reality. Ideally, an error correction block should be placed after every gate operation in a quantum circuit. This increases the overhead and reduced the speedup of the quantum circuit. Moreover, the error correction blocks themselves may induce errors as the gates used for error correction may be noisy. In this paper, we have proposed a procedure to trace error probability due to noisy gates and decoherence in quantum circuit and place an error correcting block only when the error probability exceeds a certain threshold. This procedure shows a drastic reduction in the required number of error correcting blocks. Furthermore, we have considered concatenated codes with tile structure layout lattice architecture[25][21],[24] and SWAP gate based qubit transport mechanism. Tracing errors in higher levels of concatenation shows that, in most cases, after 1 or 2 levels of concatenation, the number of QECC blocks required become static. However, since the gate count increases with increasing concatenation, the percentage saving in gate count is considerably high.

1 Introduction

Quantum computing protocols[3, 4, 2] often assume the presence of an idealised quantum system which is not in contact with its environment and hence is error free. However, it is impossible to attain such idealised situation. So error correction is necessary to allow quantum computation. Quantum error correcting codes[20, 8, 22, 11] have been proposed in the literature for this purpose. However, presence of error correcting codes does not prevent the propagation of error in a circuit. Hence a single error, by propagating to different qubits, can cause multiple errors which cannot be corrected by single error correcting codes. Shor[19] has shown that fault tolerant quantum computing is possible. Error correction, together with fault tolerance, ensures reliable quantum computation.

However, due to high error affinity of quantum states, repeated error corrections are necessary which often hinders the promised speed of computation and also increases the resource requirement. It may be possible that in small computation, the resource requirement of error correction is more than that of the computation itself. Furthermore, in real situation, the gates used in error correction circuit may be noisy and hence they themselves can incorporate errors in the circuit. Nevertheless, when error probability is low, it is unnecessary to place a QECC block after every gate operation. In this paper, we have proposed a mechanism of error tracing where an offline calculation is done beforehand to trace the error probability through the circuit. When this probability exceeds a predefined threshold, only then an error correcting block is placed. Furthermore, since this process is probabilistic, we have proposed the use fault-tolerant gates to implement error correction. This ensures that even if errors occur, their propagation in the circuit is limited. We have considered this mechanism for both linear as well as concatenated quantum circuits. In both cases the source of error is noisy gates and error due

to decoherence, which we call memory error, and Pauli error model has been considered[27].

The results of our proposed mechanism show a drastic reduction in the required number of QECC blocks, often reducing it to 0. This is, thus, a positive result for performing long quantum computations without having to worry about error correction in every step. If error probability is more, then concatenated codes[15] can be used to correct multiple errors. Even though the resource requirement for concatenation increases substantially with increasing level of concatenation, this error tracing mechanism shows that required number of QECC blocks can be reduced by an appreciable amount in concatenated codes too.

The remaining paper is organised in the following way - Section 2 gives a brief description of fault tolerance and some of the technologies used to implement a quantum computer. In Section 3, we show the calculation of gate error probability in a linear quantum circuit. Section 4 contains an efficient algorithm to calculate the precise memory error probability in a linear quantum circuit. In Section 5, we combine these two sources of errors to find the total error probability. Section 6 gives a brief review of concatenated codes and we show the application of our proposed technique in concatenated quantum circuits. In Section 7, we provide some benchmark circuits and give the result of the percentage save in QECC blocks by applying our proposed technique. We conclude this paper in Section 8.

2 Technology and Fault Tolerance

The state of a quantum system is completely described by the wavefunction Ψ . Time evolution of this wavefunction is determined by the Schrödinger equation

$$i\hbar \frac{\partial |\Psi\rangle}{\partial t} = H |\Psi\rangle$$

where \hbar is the reduced Plank's Constant $= \frac{h}{2\pi}$ and H is a hermitian operator called the *Hamiltonian* of the system. The most general idea behind quantum computation is to be able to control this Hamiltonian to perform a quantum operation. Different quantum systems have different Hamiltonians and there are also different technologies[12] used to implement the computation. An operation may be easily performed in one technology but with difficulty in another. Hence, one technology may be more suitable for implementing a quantum logic gate than another. Different technologies considered in this paper are - Ion Trap (IT)[17], Superconductor (SC)[23], Quantum Dot (QD)[26], Neutral Atom (NA)[18], Linear Photonics (LP)[10], Non Linear Photonics (NP)[14]. The primitive quantum operations realizable in each of the six technologies are shown in table 1. Since for a particular technology, the non-primitive gates have a higher cost than the primitive ones, it will be useful if after choosing a particular technology, the non-primitive gates of a quantum circuit are realized in terms of the primitive ones.

Table 1: Supported operations in different technologies[13]

Technology	One qubit operation	Two qubits operation
QD	R_x, R_z, X, Z, S, T	CZ
NA	R_{xy}	CZ
LP	$R_x, R_y, R_z, X, Y, Z, S, T, H$	CNOT, CZ, SWAP, ZENO
NP	Asqu, R_x, R_y, R_z, H	CNOT
SC	R_x, R_y, R_z	iSWAP, CP
IT	R_{xy}, R_z	G

A quantum circuit is said to be fault tolerant if it does not allow error to propagate i.e. if a single error occurs in one of the components, then the procedure will cause at most one error in each of the encoded blocks produced by the component. There exists a group of error correction codes which can be easily implemented fault-tolerantly, called CSS code[6]. Shor code[20] and Steane Code[22] fall within this group of code. It is shown in [7] and [16] that 5 qubit code[11] can also be implemented fault-tolerantly.

The lattice architectures[25],[21],[24] proposed for the error correcting codes support the implementation of gates in Clifford + T library (CTL). However, not every quantum system directly supports the CTL. This makes the implementation of fault-tolerant circuits with CTL inefficient. In [13], the authors have extended the CTL library to a larger set of gates, the fault-tolerant set (FTS), to bridge the gap between CTL and FTS. All the operations in FTS are primitive to each quantum technology and thus can be efficiently implemented. FTS for one qubit is defined as follows

$$\text{FTS}(1) = \{R_A(k, \frac{\pi}{4}), H\} \text{ where } A \in \{x, y, z\}$$

Two qubit FTS is defined as follows

$$\text{FTS}(2) = \{\text{CNOT}, \text{CZ}, \text{SWAP}, \text{ZENO}, G(\frac{\pi}{2}), G(\frac{3\pi}{2})\}$$

The elements of FTS can be trivially obtained from table 2.

Table 2: Conversion between one-qubit FTS and CTL[13]

k	R_z	R_x	R_y
1	T	HTH	$SHTHS^\dagger$
2	S	HSH	HZ
3	ZT^\dagger	$HZT^\dagger H$	$SHZT^\dagger HS^\dagger$
4	Z	X	ZX
5	ZT	$HZTH$	$SHZTHS^\dagger$
6	S^\dagger	$HS^\dagger H$	ZH
7	T^\dagger	$HT^\dagger H$	$SHT^\dagger HS^\dagger$

3 Tracing error due to noisy gate operation

One of the sources of error in a quantum circuit is noisy gates. In each technology, there are some primitive gates which can be directly implemented (see table 1). Other gates are implemented by the combination of these primitive gates. We consider that the gate error probability for the implementation of any primitive gate is w . The error probability for non-primitive gates depends on the number of primitive gates required to implement it. We present the fault-tolerant circuits of one gate in each technology considered, as obtained from FTQLS[13], and then calculate the error probability based on these fault-tolerant circuits. The actual value of w may depend on technology and experimental conditions. We have denoted the total gate error probability of the fault tolerant model of each gate by g_0 . The subscript 0 indicates that this calculation is for the 0^{th} level of concatenation.

3.1 Ion Trap

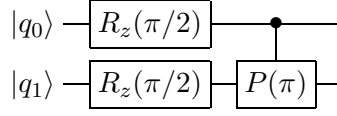
We show the gate error calculation of R_y gate in Ion Trap technology. R_y denotes rotation along y-axis. We have considered a rotation by angle π . The error probability is given as

$$|q_0\rangle \text{---} \boxed{R_z(\pi)} \text{---} \boxed{R_x(\pi)} \text{---}$$

$$\begin{aligned} g_0 &= 1 - (1 - g_{0_{R_z}})(1 - g_{0_{R_x}}) \\ &= 1 - (1 - w)(1 - w) \\ &= 1 - (1 - w)^2 \end{aligned}$$

3.2 Superconductor

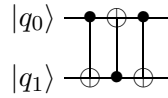
We consider Geo gate in superconductor technology. The rotation considered is $\frac{\pi}{2}$.



$$\begin{aligned} g_0 &= 1 - (1 - g_{0_{R_z}})^2 (1 - g_{0_{CP}}) \\ &= 1 - (1 - w)^2 (1 - w) \\ &= 1 - (1 - w)^3 \end{aligned}$$

3.3 Linear Photonics

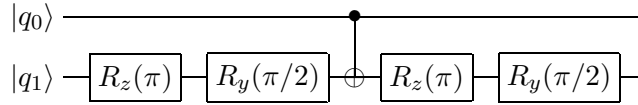
In linear photonics, SWAP gate is realised using 3 CNOT gates. The error probability is given as



$$g_0 = 1 - (1 - g_{0_{CNOT}})^3 = 1 - (1 - w)^3$$

3.4 Non Linear Photonics

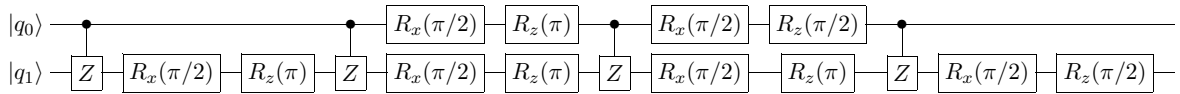
The fault tolerant model and the error probability of Controlled-Z (CZ) gate in Non Linear Photonics is



$$\begin{aligned} g_0 &= 1 - (1 - g_{0_{R_z}})^2 (1 - g_{0_{R_y}})^2 (1 - g_{0_{CNOT}}) \\ &= 1 - (1 - w)^2 (1 - w)^2 (1 - w) \\ &= 1 - (1 - w)^5 \end{aligned}$$

3.5 Quantum Dot

The fault tolerant model Zeno gate in Quantum Dot is



$$\begin{aligned} g_0 &= 1 - (1 - g_{0_{R_x}})^6 (1 - g_{0_{R_z}})^6 (1 - g_{0_{CZ}})^4 \\ &= 1 - (1 - w)^6 (1 - w)^6 (1 - w)^4 \\ &= 1 - (1 - w)^{16} \end{aligned}$$

Table 3 contains the error probability of each gate in different technologies.

4 Tracing error due to decoherence

Tracing error due to decoherence is not so trivial as noisy gate errors. This is because one requires precise calculation of how long a qubit is idle at any part of the circuit, which on other hand is dependent on the operation times of the quantum gates. Tables 4 and 5 contains the data of the time requirement for gate operation and the error probability in each technology considered respectively. We provide an efficient algorithm 1 which takes as input a .qasm file[13], divides the entire quantum circuit into time slices and calculate which slices are

Table 3: Comparative study of Gate error probability in different technologies

Gates	IT	LP	NA	NP	QD	SC
Rx	w	w	w	w	w	w
Ry	$1 - (1 - w)^2$	$1 - (1 - w)^2$	$1 - (1 - w)^2$	$1 - (1 - w)^2$	$1 - (1 - w)^3$	$1 - (1 - w)^2$
Rz	w	w	w	w	w	w
X	w	w	w	w	w	w
Y	$1 - (1 - w)^2$	$1 - (1 - w)^2$	$1 - (1 - w)^2$	$1 - (1 - w)^2$	$1 - (1 - w)^3$	$1 - (1 - w)^2$
Z	w	w	w	w	w	w
H	$1 - (1 - w)^7$	$1 - (1 - w)^7$	$1 - (1 - w)^7$	$1 - (1 - w)^7$	$1 - (1 - w)^7$	$1 - (1 - w)^7$
S	w	w	w	w	w	w
T	w	w	w	w	w	w
CNOT	$1 - (1 - w)^5$	w	$1 - (1 - w)^3$	w	$1 - (1 - w)^5$	$1 - (1 - w)^3$
CZ	$1 - (1 - w)^3$	w	w	$1 - (1 - w)^5$	w	w
SWAP	$1 - (1 - w)^{11}$	$1 - (1 - w)^3$	$1 - (1 - w)^9$	$1 - (1 - w)^3$	$1 - (1 - w)^{16}$	$1 - (1 - w)^{13}$
ZENO	$1 - (1 - w)^{10}$	$1 - (1 - w)^6$	$1 - (1 - w)^{12}$	$1 - (1 - w)^9$	$1 - (1 - w)^{16}$	$1 - (1 - w)^{10}$
GEO($\frac{\pi}{2}$)	w	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$
GEO($\frac{3\pi}{4}$)	$1 - (1 - w)^5$	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^7$	$1 - (1 - w)^7$
GEO(π)	$1 - (1 - w)^5$	$1 - (1 - w)^2$	$1 - (1 - w)^5$	$1 - (1 - w)^2$	$1 - (1 - w)^9$	$1 - (1 - w)^2$
GEO($\frac{5\pi}{4}$)	$1 - (1 - w)^5$	$1 - (1 - w)^3$	$1 - (1 - w)^5$	$1 - (1 - w)^3$	$1 - (1 - w)^9$	$1 - (1 - w)^5$
GEO($\frac{3\pi}{2}$)	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$	$1 - (1 - w)^3$

idle. Thus the problem of finding error probability due to decoherence reduces to the problem of finding idle slices. For this algorithm we have assumed that if two gates are operated one after another on a qubit, then the time lapse between them is negligible and decoherence doesn't occur in that time gap. Furthermore, we have considered that no decoherence occurs when a qubit is undergoing a gate operation.

Table 4: Gate time in ns[24]

Technology	CNOT	SWAP	H	M_x	M_z	X	Y	Z	S	T
QD	27	81	12	100	112	10	11	1	1	1
NA	2533	7599	781	80457	80000	457	457	915	915	915
LP	10	10	1	2	1	1	1	1	1	1
NLP	12	36	151	50	1	1	1	1	1	1
SC	26	13	16	10	26	10	10	1	1	1
IT	120000	10000	6000	106000	100000	500	500	3000	2000	1000

Table 5: Probability of error of worst gate and memory error in different technology[24]

Technology	Probability of Gate error	Memory error (per ns)
QD	9.89×10^{-1}	3.47×10^{-2}
NA	8.12×10^{-3}	0.00
LP	1.01×10^{-1}	9.80×10^{-4}
NLP	5.20×10^{-3}	9.80×10^{-5}
SC	1.00×10^{-5}	1.00×10^{-5}
IT	3.19×10^{-9}	2.52×10^{-12}

FTQLS[13] breaks down any multi-qubit gate into one or two qubit gates. Hence we need not worry about gates involving more qubits. We consider a simple circuit shown in figure 1 and the technology to be quantum dot. We shall use algorithm 1 to calculate the memory error probability for each qubit in this circuit.

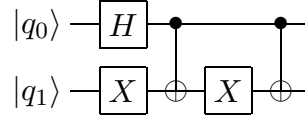
Algorithm 1: Memory error calculation

input : *.qasm* file containing the fault tolerant model of the required circuit as obtained from FTQLS

output: The placement of the gates and the idle regions

```
1 begin
2    $level \leftarrow$  list containing the current level of each qubit;
3    $level[i] \leftarrow 0$  for all  $i$ ;
4    $slice \leftarrow$  GCD of the gate operation time of all the gates in the used PMD;
5   for each line in .qasm file do
6     if one qubit gate then
7        $l \leftarrow level[i]$ , current level of qubit on which the gate operates;
8       Place the gate in level  $l + 1$ ;
9        $s \leftarrow$  gate operation time;
10       $sn \leftarrow s/slice$ ;
11      /*  $sn$  contains the number of slices required */
12       $level[i] = l + sn - 1$ ;
13      /* -1 since the gates are placed at the current level + 1 */
14    else
15       $l \leftarrow \max\{level[i], level[j]\}$ ;
16      Place the gate in level  $l + 1$  of both the qubits;
17       $s \leftarrow$  gate operation time;
18       $sn \leftarrow s/slice$ ;
19       $level[i], level[j] = l + sn - 1$ ;
```

Figure 1: Example quantum circuit



The steps for memory error calculation are as follows

- $slice = 1$ (GCD of time operations for QD gates from Table 4)
- Place H in level 1 ($0 + 1$) of qubit $|q_0\rangle$ and X in level 1 of qubit $|q_1\rangle$.
- Gate operation time for H is $s_H = 12$ and that of X is $s_X = 10$.
- Number of slices required for $|q_0\rangle$ is 12 and that of $|q_1\rangle$ is 10.
- New $level$ of $|q_0\rangle$ is 12 and new $level$ of $|q_1\rangle$ is 10.
- CNOT is a 2 qubit gate. So $l \leftarrow \max\{12, 10\} = 12$.
- Place CNOT in level $l + 1 = 13$ for both qubits.
- Qubit $|q_1\rangle$ is idle for 2ns.
- CNOT acts for 27ns. So new level of both qubits is $13 + 27 - 1 = 39$.
- Place gate X at level 40 for qubit $|q_1\rangle$.
- X acts for 10ns. So new level of $|q_1\rangle$ is $40 + 10 - 1 = 49$.
- CNOT is a 2 qubit gate. So $l \leftarrow \max\{39, 49\} = 49$.
- Place CNOT in level 50 for both qubits.

- Qubit $|q_0\rangle$ is idle for 10ns.

Thus after the placement of gates according to the algorithm, we see qubit $|q_0\rangle$ has been idle for 10ns while qubit $|q_1\rangle$ has been idle for 2ns. The memory error probability per ns for QD is 3.47×10^{-2} . So the error probability in $|q_1\rangle$ is $1 - (1 - 3.47 \times 10^{-2})^2 = 0.068$. Here $(1 - 3.47 \times 10^{-2})$ is the probability of no error in 1ns. Squaring it gives us the probability of no error for 2ns. Finally we subtract it from 1 to have the error probability in 2ns.

Similarly, the error probability for qubit $|q_0\rangle$ is $1 - (1 - 3.47 \times 10^{-2})^{10} = 0.3$. This calculation can be used for simulation before the actual implementation of the quantum circuit.

5 Error tracing in linear quantum circuit

Calculation of gate error probability for different gates in each technology and tracing memory error have already been taken up individually in the previous sections. Using these two together allows us to trace the total error probability in a linear quantum circuit. We consider again the circuit in figure 1 to show the steps for error tracing. This calculation is done completely algebraically to make it independent of any technology. The gate error probability for primitive gates is w as before and the probability of *no memory error* for each idle slice is w_0 .

- For $|q_0\rangle$, the probability of no error for H is $(1 - w)^7$.
- For $|q_1\rangle$, the probability of no error for X is $(1 - w)$.
- From the algorithm to find memory error, we have seen that there are 2 idle slices after X while H is still operating. So the probability of no memory error for two slices is w_0^2 .
- Total probability of no error for $|q_1\rangle$ upto this is $w_0^2(1 - w)$.
- Since CNOT is a 2 qubit gate, we need to update the error probability of both qubits to the maximum of the error probabilities of the qubits. Since w and w_0 are both fractions $\ll 1$ and we assume $w_0 \ll w$, we take that $(1 - w)^7 < w_0^2(1 - w)$ (this can change according to actual value of w and w_0). If $(1 - w)^7 < w_0^2(1 - w)$, then the error probability of $|q_0\rangle$ is more than that of $|q_1\rangle$. So we update the error probability of both qubits as $1 - (1 - w)^7$.
- Present probability of no error in both qubits is $(1 - w)^7$.
- No error probability of CNOT is $(1 - w)^5$. Hence no error probability of both qubits is $(1 - w)^5(1 - w)^7 = (1 - w)^{12}$.
- Qubit $|q_0\rangle$ is now idle for 10ns. So probability of no memory error is w_0^{10} .
- Therefore total probability of no error in $|q_0\rangle$ is $w_0^{10}(1 - w)^{12}$.
- Probability of no error while X operates on $|q_1\rangle$ is $(1 - w)$.
- Therefore total probability of no error in $|q_1\rangle$ is $(1 - w)^{13}$.
- Again considering $w_0 \ll w$, we conclude that $(1 - w)^{13} < w_0^{10}(1 - w)^{12}$.
- Hence the error probability is more for $|q_1\rangle$.
- Since CNOT is a two qubit gate, minimum of the no error probability, i.e. $(1 - w)^{13}$ or maximum of the error probability, i.e. $1 - (1 - w)^{13}$ is assigned to both the qubits.
- Finally, the total error probability of both $|q_0\rangle$ and $|q_1\rangle$ is $1 - (1 - w)^{13}$.

Since this calculation is dependent on the actual values of w and w_0 , the inequality assumptions in steps 5 and 12 may change according to the original values. When the error probability exceeds a pre-defined threshold, we place an error correcting block. The new error probability of the qubits involved is updated to the error probability of the error correcting block.

6 Error tracing in higher concatenation level

6.1 Concatenated code

Though different quantum error correcting codes[20, 22, 11] are available in the literature, all these codes assume that the error probability of the quantum channel is low and only a single error can occur. If more than one error occurs, then these codes fail. It is possible to use Stabilizers[8] to formulate a code which can correct t errors in a system. However, the resource requirement increases largely with the value of t and even that code fails if $t + 1$ errors occur. The solution to this problem is concatenation[15].

The information of a single qubit can be protected by distributing it into n qubits. This forms an n qubit error correcting code. We can consider these n physical qubits as a single logical qubit. This logical qubit can again be encoded for error correction using the same or different code. This system is now able to correct 2 errors. By increasing the levels of concatenation in similar way, one can correct any arbitrary number of errors. Further details on concatenated code is available in [15].

6.2 Tracing of error in higher concatenation

In sections 3, 4 & 5, we have considered linear circuit, i.e. concatenation level 0. Now, we study the effect of higher concatenation on the error probability. To calculate the error for higher concatenation, an underlying structure for the gate operations is required. We have considered a 2-D nearest neighbour lattice architecture using logical noisy SWAP gates as the basic qubit transport mechanism[25, 21]. In a concatenated architecture, after first level of encoding each physical qubit is replaced by a 2-D block or cell or tile, that forms the logical qubit. After the second level of encoding each such cell is replaced by a 2-D block of such logical qubit cells, and so on. We have considered the tile architecture for the physical layout of Bacon-Shor code[1, 21], Steane code[22, 25] and Knill's code[24]. To the best of our knowledge, the tile structures are possible for the gates in the CTL library or any gate which can be obtained in a compound way from one or more operations in the CTL library.

In higher levels of concatenation, when a gate is operated on a logical qubit, some of the qubits in the lower level(s) of concatenation can remain idle even when the gate is operating. So the assumption that during gate operation decoherence cannot occur, does not hold good for higher concatenation level. Let g_n be the gate error at the n th level of encoding, g_{k_A} is the error probability of gate A at k -th level of encoding. Similarly let t_n be the gate delay at the n -th level of encoding, t_{k_A} is the delay of gate A at k -th level of encoding. An error correcting code which can correct a single error fails if two errors occur on the system. For each logical block, probability of failure is

$$Prob(\text{at least two errors per logical block}) = 1 - Prob(\text{no gate fails}) - Prob(\text{exactly one gate fails})$$

For higher levels of encoding, we consider the failure probability of gates at the next lower level.

Gate error probability in a linear quantum circuit was dependent on the technology used. However, the tile architecture is different for different QECC and hence error probability at the logical level depends on the QECC used and not on the technology. We show the operation of vertical CNOT gate operation in Knill code 5×5 tile structure in Figure 2 and demonstrate the calculation of error. In the figure, $|q\rangle$ represent the set of control qubits and $|d\rangle$ represent the set of target qubits. From `reffig:conc` we can see that the logical CNOT gate at n^{th} level requires 24 SWAP gates and 4 CNOT gates at $(n-1)^{th}$ level. Of these, failure of any one causes errors in at least two qubits. Thus to check the total error probability we need to consider the probability of failure of each gate individually and also both at the same time. Hence the probability of failure at the n^{th} level of encoding is

$$g_n = 1 - (1 - g_{n-1_{SWAP}})^{24}(1 - g_{n-1_{CNOT}})^4 - \binom{4}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^3 - \binom{24}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{23} (1 - g_{n-1_{CNOT}})^4 \quad (1)$$

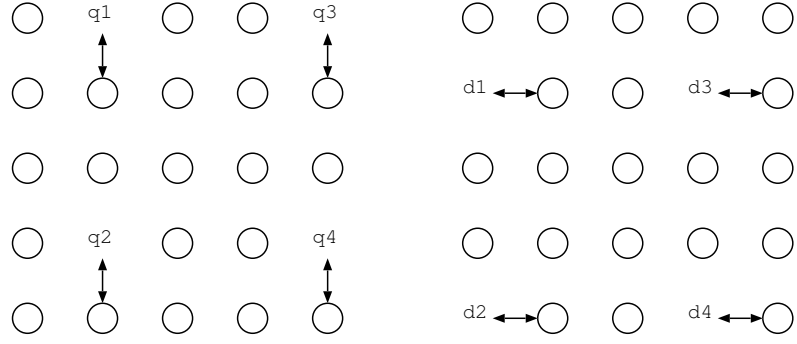
In Tables 7 and 6, we present the algebraic expressions for the error probability of the logical qubits for various gates in concatenation.

Table 6: Error probability of FTS(2) gates at logical level for each QECC

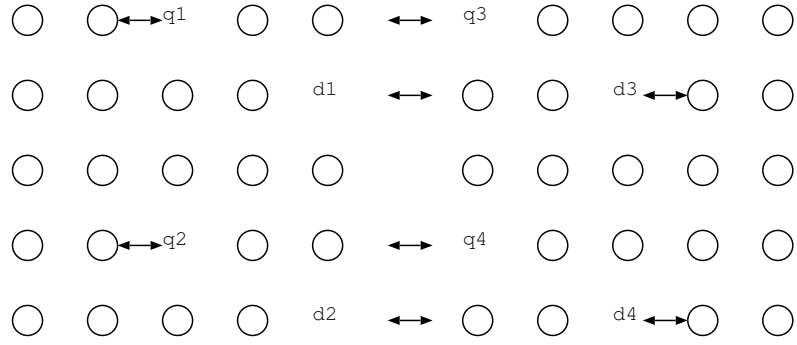
Gates	Bacon-Shor	Steane	Knill
SWAP	$1 - (1 - g_{n-1_{SWAP}})^{33} - \binom{12}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{32}$	$1 - [(1 - g_{n-1_{SWAP}})^{26} + 8g_{n-1_{SWAP}} \binom{1}{1} g_{n-1_{SWAP}}^{25}] (1 - M_{n_{SWAP}} - M_{n_{SWAP}} (1 - g_{n-1_{SWAP}})^{26})$	$1 - [(1 - g_{n-1_{SWAP}})^{40} + \binom{32}{1} g_{n-1_{SWAP}} (1 - [(1 - g_{n-1_{SWAP}})^{39}]) (1 - M_{n_{SWAP}} - M_{n_{SWAP}} (1 - g_{n-1_{SWAP}})^{40})]$
CNOT	$1 - (1 - g_{n-1_{CNOT}})^9 (1 - g_{n-1_{SWAP}})^{54} - \binom{36}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{CNOT}})^9 (1 - g_{n-1_{SWAP}})^{53} - \binom{9}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{CNOT}})^8 (1 - g_{n-1_{SWAP}})^{54}$	$1 - [(1 - g_{n-1_{SWAP}})^{43} (1 - g_{n-1_{CNOT}})^7 + \binom{26}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_{CNOT}})^7 + \binom{7}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{43} (1 - g_{n-1_{CNOT}})^6] (1 - M_{n_{CNOT}} - M_{n_{CNOT}} (1 - g_{n-1_{SWAP}})^{43} (1 - g_{n-1_{CNOT}})^7)$	$1 - (1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^4 - \binom{4}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^3 - \binom{24}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{23} (1 - g_{n-1_{CNOT}})^4$
CZ	$1 - (1 - g_{n_H})(1 - g_{n_{CNOT}})$	$1 - (1 - g_{n_H})(1 - g_{n_{CNOT}})$	$1 - (1 - g_{n_H})(1 - g_{n_{CNOT}})$
G	$1 - (1 - g_{n_S})^2 (1 - g_{n_H})(1 - g_{n_{CNOT}})$	$1 - (1 - g_{n_S})^2 (1 - g_{n_H})(1 - g_{n_{CNOT}})$	$1 - (1 - g_{n_S})^2 (1 - g_{n_H})(1 - g_{n_{CNOT}})$
ZENO	$1 - (1 - g_{n_S})^2 (1 - g_{n_{SWAP}})(1 - g_{n_{CZ}})$	$1 - (1 - g_{n_S})^2 (1 - g_{n_{SWAP}})(1 - g_{n_{CZ}})$	$1 - (1 - g_{n_S})^2 (1 - g_{n_{SWAP}})(1 - g_{n_{CZ}})$

Figure 2: An encoded CNOT operation between $|d1, d2, d3, d4\rangle$ (target) and $|q1, q2, q3, q4\rangle$ (control) in Knill code 5×5 tile architecture

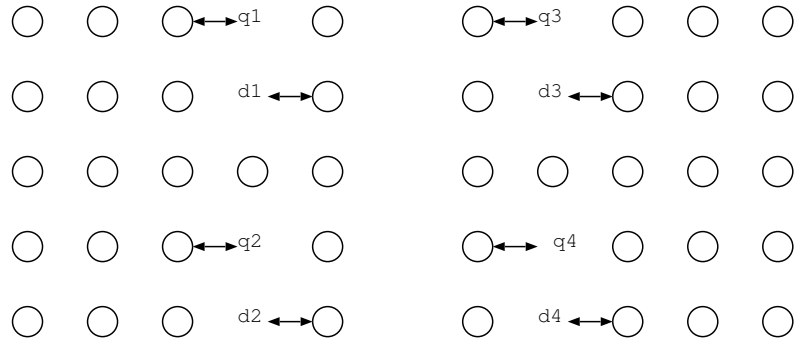
Time Step 1:



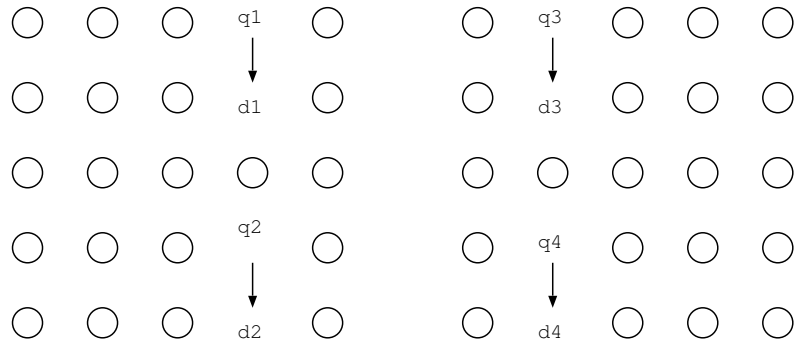
Time Step 2:



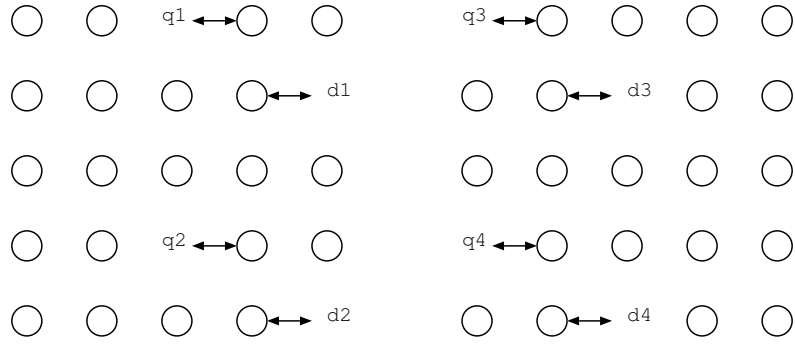
Time Step 3:



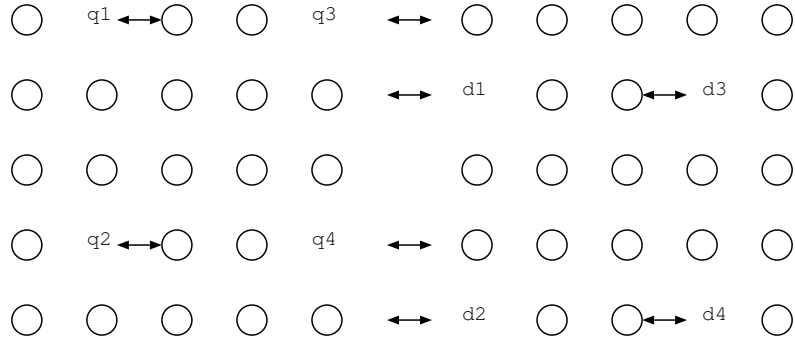
Time Step 4:



Time Step 5:



Time Step 6:



Time Step 7:

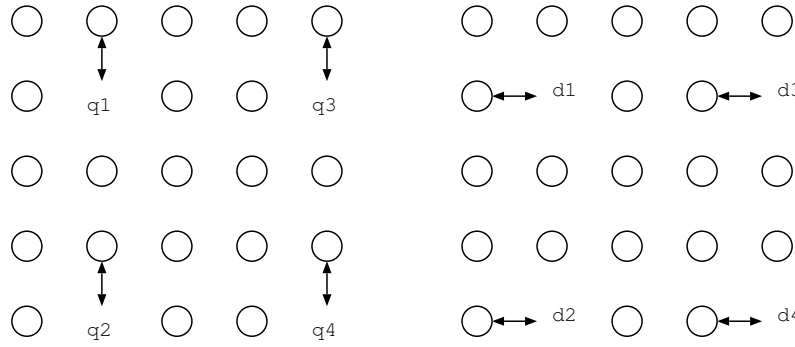


Table 7: Error probability of FTS(1) gates at logical level for each QECC

Gates	Bacon-Shor	Steane	Knill
X	$1 - (1 - g_{n-1_X})^9 - \binom{9}{1} g_{n-1_X} (1 - g_{n-1_X})^8$	$1 - (1 - g_{n-1_X})^7 - \binom{7}{1} g_{n-1_X} (1 - g_{n-1_X})^6$	$1 - (1 - g_{n-1_X})^2 - \binom{2}{1} g_{n-1_X} (1 - g_{n-1_X})$
Y	$1 - (1 - g_{n-1_Y})^9 - \binom{9}{1} g_{n-1_Y} (1 - g_{n-1_Y})^8$	$1 - (1 - g_{n-1_Y})^7 - \binom{7}{1} g_{n-1_Y} (1 - g_{n-1_Y})^6$	$1 - (1 - g_{n-1_Y})(1 - g_{n-1_X})(1 - g_{n-1_Z}) - g_{n-1_Y}(1 - g_{n-1_X})(1 - g_{n-1_Z}) - g_{n-1_X}(1 - g_{n-1_Y})(1 - g_{n-1_Z}) - g_{n-1_Z}(1 - g_{n-1_X})(1 - g_{n-1_Y})$
Z	$1 - (1 - g_{n-1_Z})^9 - \binom{9}{1} g_{n-1_Z} (1 - g_{n-1_Z})^8$	$1 - (1 - g_{n-1_Z})^7 - \binom{7}{1} g_{n-1_Z} (1 - g_{n-1_Z})^6$	$1 - (1 - g_{n-1_Z})^2 - \binom{2}{1} g_{n-1_Z} (1 - g_{n-1_Z})$
H	$1 - (1 - g_{n-1_H})^9 (1 - g_{n-1_{SWAP}})^{32} (1 - M_{n_H}) - g_{n-1_H} (1 - g_{n-1_H})^8 (1 - g_{n-1_{SWAP}})^{32} (1 - M_{n_H}) - M_{n_H} (1 - g_{n-1_H})^9 (1 - g_{n-1_{SWAP}})^{32}$	$1 - (1 - g_{n-1_H})^7 - \binom{7}{1} g_{n-1_H} (1 - g_{n-1_H})^6$	$1 - (1 - g_{n-1_H})^4 - \binom{4}{1} g_{n-1_H} (1 - g_{n-1_H})^3$
S	$1 - [(1 - g_{n-1_H})^9 (1 - g_{n-1_{CNOT}})^9 (1 - g_{n-1_{SWAP}})^{42} + \binom{21}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{41} (1 - g_{n-1_H})^9 (1 - g_{n-1_{CNOT}})^9 + \binom{9}{1} g_{n-1_H} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_H})^8 (1 - g_{n-1_{CNOT}})^9 + \binom{9}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_H})^9 (1 - g_{n-1_{CNOT}})^8] (1 - M_{n_S}) - M_{n_S} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_H})^9 (1 - g_{n-1_{CNOT}})^9$	$1 - (1 - g_{n-1_S})^7 (1 - g_{n-1_Z})^7 - \binom{7}{1} g_{n-1_S} (1 - g_{n-1_S})^6 (1 - g_{n-1_Z})^7$	$1 - [(1 - g_{n-1_{SWAP}})^{20} (1 - g_{n-1_{CNOT}})^4 (1 - g_{n-1_H})^4 + \binom{16}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{19} (1 - g_{n-1_{CNOT}})^4 (1 - g_{n-1_H})^4 + \binom{4}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{20} (1 - g_{n-1_{CNOT}})^3 (1 - g_{n-1_H})^4 + \binom{4}{1} g_{n-1_H} (1 - g_{n-1_{SWAP}})^{20} (1 - g_{n-1_{CNOT}})^4 (1 - g_{n-1_H})^3] (1 - M_{n_S}) - M_{n_S} (1 - g_{n-1_{SWAP}})^{20} (1 - g_{n-1_{CNOT}})^4 (1 - g_{n-1_H})^4$
T	$1 - [(1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_{CNOT}})^{18} (1 - g_{n-1_H})^9 (1 - g_{n-1_{M_z}})^9 + \binom{21}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{41} (1 - g_{n-1_{CNOT}})^{18} (1 - g_{n-1_H})^9 (1 - g_{n-1_{M_z}})^9 + \binom{18}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_{CNOT}})^{17} (1 - g_{n-1_H})^9 (1 - g_{n-1_{M_z}})^9 + \binom{9}{1} g_{n-1_H} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_{CNOT}})^{18} (1 - g_{n-1_H})^7 (1 - g_{n-1_{M_z}})^9 + \binom{9}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_{CNOT}})^{18} (1 - g_{n-1_H})^9 (1 - g_{n-1_{M_z}})^8] (1 - M_{n_T}) - M_{n_T} (1 - g_{n-1_{SWAP}})^{42} (1 - g_{n-1_{CNOT}})^{18} (1 - g_{n-1_H})^9 (1 - g_{n-1_{M_z}})^9$	$1 - [(1 - g_{n-1_{SWAP}})^{40} (1 - g_{n-1_{CNOT}})^7 (1 - g_{n-1_X})^7 (1 - g_{n-1_S})^7 (1 - g_{n-1_{M_z}})^7 + \binom{22}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{39} (1 - g_{n-1_{CNOT}})^7 (1 - g_{n-1_X})^7 (1 - g_{n-1_S})^7 (1 - g_{n-1_{M_z}})^7 + \binom{7}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{40} (1 - g_{n-1_{CNOT}})^6 (1 - g_{n-1_X})^7 (1 - g_{n-1_S})^7 (1 - g_{n-1_{M_z}})^7 + \binom{7}{1} g_{n-1_{M_z}} (1 - g_{n-1_{SWAP}})^{40} (1 - g_{n-1_{CNOT}})^7 (1 - g_{n-1_X})^7 (1 - g_{n-1_S})^7 (1 - g_{n-1_{M_z}})^6 + \binom{7}{1} g_{n-1_X} (1 - g_{n-1_{SWAP}})^{40} (1 - g_{n-1_{CNOT}})^7 (1 - g_{n-1_X})^7 (1 - g_{n-1_S})^7 (1 - g_{n-1_{M_z}})^7 + \binom{7}{1} g_{n-1_S} (1 - g_{n-1_{SWAP}})^{40} (1 - g_{n-1_{CNOT}})^7 (1 - g_{n-1_X})^7 (1 - g_{n-1_S})^7 (1 - g_{n-1_{M_z}})^7]$	$1 - [(1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^8 (1 - g_{n-1_H})^4 (1 - g_{n-1_{M_z}})^4 + \binom{20}{1} g_{n-1_{SWAP}} (1 - g_{n-1_{SWAP}})^{23} (1 - g_{n-1_{CNOT}})^8 (1 - g_{n-1_H})^4 (1 - g_{n-1_{M_z}})^4 + \binom{8}{1} g_{n-1_{CNOT}} (1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^7 (1 - g_{n-1_H})^4 (1 - g_{n-1_{M_z}})^4 + \binom{4}{1} g_{n-1_H} (1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^8 (1 - g_{n-1_H})^3 (1 - g_{n-1_{M_z}})^4 + \binom{4}{1} g_{n-1_{M_z}} (1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^8 (1 - g_{n-1_H})^4 (1 - g_{n-1_{M_z}})^3] (1 - M_{n_T}) - M_{n_T} (1 - g_{n-1_{SWAP}})^{24} (1 - g_{n-1_{CNOT}})^8 (1 - g_{n-1_H})^4 (1 - g_{n-1_{M_z}})^4$

7 Benchmark results

We have applied our proposed technique of error tracing on various benchmark circuits. For each circuit, we have considered a linear case (concatenation 0) and concatenation level up to 4. Furthermore, for the concatenation codes, we have considered Bacon-Shor, Steane and Knill's code tile architecture for each gate and have varied the threshold as 0.001, 0.01 and 0.1 and have shown the percentage saving in each case.

Results of various benchmark circuits are shown in Table 8 - Table ???. From the values, a few analysis can be made as follows -

- Ion Trap shows an extremely good result with 100% savings in lower concatenation levels. Even in higher concatenation levels, the savings are always close to 100%. However, changing the error threshold does not seem to have much effect in this technology. This is because, the gate error probability in this technology (Table 5) is of the order of 10^{-12} , which is quite lower than the lowest threshold we have considered (10^{-3}). For this reason, this technique gives equivalent results in all the three thresholds.
- Superconductor gives the second best result. Since the error probability in this technology (refer Table 5) is more than that of Ion Trap, the savings in this technology is less. Nevertheless, the savings are still near 100% in most cases. In this technology, both the gate error probability and memory error probability is of the order of 10^{-5} . So when considering both, the error probability becomes comparable to our thresholds. So here we see that the results are better for higher threshold values.
- Linear Photonics and Quantum Dot show the worst results when our technique is used. Such results are expected since for LP the gate error probability and memory error probability are of the orders of 10^{-1} and 10^{-4} respectively and for Quantum Dot they are of the orders of 10^{-1} and 10^{-2} respectively. We have considered thresholds 10^{-3} , 10^{-2} & 10^{-1} . Since the error probabilities in these two technologies are always greater than our considered threshold, the results are not very positive in the linear case. However, in higher concatenation levels, there are still much savings.
- In Non Linear Photonics, the gate error probability is of the order 10^{-3} and the memory error probability is of the order 10^{-5} . Thus, the first threshold, which is 10^{-3} cannot provide savings in the linear case as it is same as the gate error probability. However, we see a much better result when the threshold is increased.
- Neutral atom is similar to Non Linear photonics since its gate error probability is also 10^{-3} . Similar analysis show that the result will not be very positive in threshold 0.001 but for higher thresholds, savings are observed in the results.
- For higher concatenation level, memory error plays a big role. This is because even when some gate is operating, qubits in the lower level of concatenation may be idle. This is the reason why with increasing levels of concatenation, the number of required QECC blocks increases initially. However, in higher concatenations, a balance is reached between the idle qubits and the qubits undergoing gate operation in different levels. So, in most cases, the required number of blocks attains an equilibrium. In some tile structures, in higher levels of concatenation, the required number of blocks even decreases. This depends solely on whether some gate is idle or not at any level of concatenation.

8 Conclusion

In this paper, we have introduced a novel technique of error tracing to reduce the required number of error correcting block in any quantum circuit. Pauli errors have been considered. The source of error in any quantum circuit is due to noisy gate and interaction with the environment. We have dealt with these two individually and have provided an efficient algorithm to determine the time for which some qubit(s) are idle while others are undergoing gate operation. The calculation of total error probability for any linear quantum circuit has also been shown.

We have, then, considered concatenated codes. The error probability in a linear quantum circuit depends on the gate error and memory error probability. But for concatenated codes, the error probability is largely dependent on the underlying lattice architecture. We have considered the architectures for Bacon-Shor code, Steane Code and Knill Code and have shown the error calculations in each case. The results from the benchmark circuits show that this technique is extremely useful for those technologies where error probability is low, for example, Ion Trap and Superconductor. However, even for other technologies, where this technique does not yield good results in the linear case, a huge amount of savings in the resource is obtainable for concatenated codes. Hence, our results show that it is possible to perform quantum computation in an open environment with much less resource requirement than the ideal case.

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Table 8: Savings on EC blocks for 3 qubit Bernstein Vazirani Search circuit[5]

Tech	QECC	Concat	Orig	Th = 0.001	% save	Th = 0.01	% save	Th = 0.1	% save
IT	BS	0	22	0	100%	0	100%	0	100%
		1	198	0	100%	0	100%	0	100%
		2	1782	15	99.16%	15	99.16%	15	99.16%
		3	16038	15	99.9%	15	99.9%	15	99.9%
		4	144342	17	99.98%	8	99.99%	0	100%
	S	0	22	0	100%	0	100%	0	100%
		1	154	0	100%	0	100%	0	100%
		2	1078	0	100%	0	100%	0	100%
		3	7546	0	100%	0	100%	0	100%
		4	52822	0	100%	0	100%	0	100%
	K	0	22	0	100%	0	100%	0	100%
		1	88	0	100%	0	100%	0	100%
		2	352	15	95.7%	15	95.7%	15	95.7%
		3	1408	15	98.9%	15	98.9%	15	98.9%
		4	5632	15	99.7%	15	99.7%	15	99.7%
SC	BS	0	20	0	100%	0	100%	0	100%
		1	180	3	98.3%	0	100%	0	100%
		2	1620	17	98.9%	14	99.1%	12	99.2%
		3	14580	17	99.88%	17	99.88%	11	99.9%
		4	131220	17	99.98%	17	99.98%	17	99.98%
	S	0	20	0	100%	0	100%	0	100%
		1	140	0	100%	0	100%	0	100%
		2	980	2	99.79%	2	99.79%	2	99.79%
		3	6860	2	99.97%	2	99.97%	2	99.97%
		4	48020	2	99.99%	2	99.99%	2	99.99%
	K	0	20	0	100%	0	100%	0	100%
		1	80	0	100%	0	100%	0	100%
		2	320	14	95.6%	14	95.6%	12	96.2%
		3	1280	14	98.9%	14	98.9%	14	98.9%
		4	5120	14	99.7%	14	99.7%	14	99.7%
LP	BS	0	22	21	4.5%	21	4.5%	21	4.5%
		1	198	21	89.4%	21	89.4%	21	89.4%
		2	1782	21	98.8%	21	98.8%	21	98.8%
		3	16038	21	99.8%	21	99.8%	21	99.8%
		4	144342	21	99.98%	21	99.98%	21	99.98%
	S	0	22	21	4.5%	21	4.5%	21	4.5%
		1	154	21	86.3%	21	86.3%	21	86.3%
		2	1078	21	98%	21	98%	21	98%
		3	7546	21	99.7%	21	99.7%	21	99.7%
		4	52822	21	99.9%	21	99.9%	21	99.9%
	K	0	22	21	4.5%	21	4.5%	21	4.5%
		1	88	21	76.1%	21	76.1%	21	76.1%
		2	352	21	94%	21	94%	21	94%
		3	1408	21	98.5%	21	98.5%	21	98.5%
		4	5632	21	99.6%	21	99.6%	21	99.6%
NP	BS	0	22	21	4.5%	9	59%	0	100%
		1	198	19	90.4%	19	90.4%	19	90.4%
		2	1782	19	98.9%	19	98.9%	19	98.9%
		3	16038	19	99.88%	19	99.88%	19	99.88%
		4	144342	19	99.98%	19	99.98%	19	99.98%
	S	0	22	21	4.5%	9	59%	0	100%
		1	154	19	87.66%	4	97.4%	2	98.7%
		2	1078	4	99.6%	2	99.8%	2	99.8%
		3	7546	2	99.97%	2	99.97%	2	99.97%
		4	52822	2	99.99%	2	99.99%	2	99.99%
	K	0	22	21	4.5%	9	59%	0	100%
		1	88	14	84%	14	84%	6	93.1%
		2	352	14	96%	14	96%	14	96%
		3	1408	14	99%	14	99%	14	99%
		4	5632	14	99.7%	14	99.7%	14	99.7%
NA	BS	0	20	19	5%	8	60%	1	95%
		1	180	19	89.4%	17	90.5%	17	90.5%
		2	1620	17	98.9%	17	98.9%	17	98.9%
		3	14580	17	99.88%	17	99.88%	17	99.88%
		4	131220	17	99.99%	17	99.99%	17	99.99%
	S	0	20	19	5%	8	75%	1	95%
		1	140	19	93.57%	11	92.1%	2	98.57%
		2	980	18	98.16%	3	99.69%	2	99.79%
		3	6860	2	99.97%	2	99.97%	2	99.97%
		4	48020	2	99.99%	2	99.99%	2	99.99%
	K	0	20	19	5%	8	60%	1	95%
		1	80	17	78.75%	14	82.5%	14	82.5%
		2	320	14	95.6%	14	95.6%	14	95.6%
		3	1280	14	98.9%	14	98.9%	14	98.9%
		4	5120	14	99.7%	14	99.7%	14	99.7%
QD	BS	0	24	23	4.2%	23	4.2%	23	4.2%
		1	216	23	89.35%	23	89.35%	23	89.35%
		2	1944	23	98.8%	23	98.8%	23	98.8%
		3	17496	23	99.87%	23	99.87%	23	99.87%
		4	157464	23	99.98%	23	99.98%	23	99.98%
	S	0	24	23	4.2%	23	4.2%	23	4.2%
		1	168	23	86.3%	23	86.3%	23	86.3%
		2	1176	23	98%	23	98%	23	98%
		3	8232	23	99.72%	23	99.72%	23	99.72%
		4	57624	23	99.96%	23	99.96%	23	99.96%
	K	0	24	23	4.2%	23	4.2%	23	4.2%
		1	96	23	76%	23	76%	23	76%
		2	384	23	94%	23	94%	23	94%
		3	1536	23	98.5%	23	98.5%	23	98.5%
		4	6144	23	99.62%	23	99.62%	23	99.62%

Table 9: Savings on EC blocks for 4 qubit Quantum Fourier Transform circuit[15]

Tech	QECC	Concat	Orig	Th = 0.001	% save	Th = 0.01	% save	Th = 0.1	% save
IT	BS	0	199	0	100%	0	100%	0	100%
		1	1791	0	100%	0	100%	0	100%
		2	16119	182	98.87%	182	98.87%	182	98.87%
		3	145071	182	99.87%	182	99.87%	182	99.87%
		4	1305639	186	99.98%	186	99.98%	186	99.98%
	S	0	199	0	100%	0	100%	0	100%
		1	1393	0	100%	0	100%	0	100%
		2	9751	182	98.1%	182	98.1%	182	98.1%
		3	68257	182	99.73%	182	99.73%	182	99.73%
		4	477799	182	99.96%	182	99.96%	182	99.96%
	K	0	199	0	100%	0	100%	0	100%
		1	796	0	100%	0	100%	0	100%
		2	3184	182	94.28%	182	94.28%	182	94.28%
		3	12736	182	98.57%	182	98.57%	182	98.57%
		4	50944	182	99.64%	182	99.64%	182	99.64%
SC	BS	0	261	5	98.08%	0	100%	0	100%
		1	2349	119	94.93%	15	99.36%	0	100%
		2	21141	260	98.77%	250	98.81%	244	98.84%
		3	190269	260	99.86%	260	99.86%	260	99.89%
		4	1712421	260	99.98%	260	99.98%	260	99.98%
	S	0	261	5	98.08%	0	100%	0	100%
		1	1827	52	97.15%	6	99.67%	0	100%
		2	12789	256	97.99%	256	97.99%	256	97.99%
		3	89523	256	99.71%	256	99.71%	256	99.71%
		4	626661	256	99.96%	256	99.96%	256	99.96%
	K	0	261	5	98.08%	0	100%	0	100%
		1	1044	20	98.08%	3	99.71%	0	100%
		2	4176	256	93.87%	256	93.87%	244	94.15%
		3	16704	256	98.47%	256	98.47%	256	98.47%
		4	66816	256	99.62%	256	99.62%	256	99.62%
LP	BS	0	234	233	0.4%	233	0.4%	233	0.4%
		1	2106	233	88.93%	233	88.93%	233	88.93%
		2	18954	233	98.77%	233	98.77%	233	98.77%
		3	170586	233	99.86%	233	99.86%	233	99.86%
		4	1535274	233	99.98%	233	99.98%	233	99.98%
	S	0	234	233	0.4%	233	0.4%	233	0.4%
		1	1638	233	85.77%	233	85.77%	233	85.77%
		2	11466	233	97.97%	233	97.97%	233	97.97%
		3	80262	233	99.71%	233	99.71%	233	99.71%
		4	561834	233	99.96%	233	99.96%	233	99.96%
	K	0	234	233	0.4%	233	0.4%	233	0.4%
		1	936	233	75.1%	233	75.1%	229	75.53%
		2	3744	233	93.77%	233	93.77%	229	93.88%
		3	14976	233	98.44%	229	98.47%	299	98.47%
		4	59904	229	99.61%	229	99.61%	299	99.61%
NP	BS	0	234	233	0.4%	117	50%	15	93.59%
		1	2106	233	88.93%	233	88.93%	233	88.93%
		2	18954	233	98.77%	233	98.77%	233	98.77%
		3	170586	233	99.86%	233	99.86%	233	99.86%
		4	1535274	233	99.98%	233	99.98%	233	99.98%
	S	0	234	233	0.4%	117	50%	15	93.59%
		1	1638	233	85.77%	229	86.02%	229	86.02%
		2	11466	229	98%	229	98%	229	98%
		3	80262	229	99.71%	229	99.71%	229	99.71%
		4	561834	229	99.96%	229	99.96%	229	99.96%
	K	0	234	233	0.4%	117	50%	15	93.59%
		1	936	229	75.53%	229	75.53%	118	49.57%
		2	3744	229	93.88%	229	93.88%	229	93.88%
		3	14976	229	98.47%	229	98.47%	229	98.47%
		4	59904	229	99.62%	229	99.62%	229	99.62%
NA	BS	0	238	237	0.42%	117	50.84%	18	92.44%
		1	2142	237	88.93%	237	88.93%	237	88.93%
		2	19278	237	98.77%	237	98.77%	237	98.77%
		3	173502	237	99.86%	237	99.86%	237	99.86%
		4	1561518	237	99.98%	237	99.98%	237	99.98%
	S	0	238	237	0.42%	117	50.84%	18	92.44%
		1	1666	237	85.77%	235	85.89%	228	86.31%
		2	11662	237	97.97%	228	98.04%	228	98.04%
		3	128282	228	99.82%	228	99.82%	228	99.82%
		4	897974	228	99.97%	228	99.97%	228	99.97%
	K	0	238	237	0.42%	117	50.84%	18	92.44%
		1	952	237	75.1%	230	75.84%	230	75.84%
		2	3808	230	93.96%	230	93.96%	230	93.96%
		3	15232	230	98.49%	230	98.49%	230	98.49%
		4	60928	230	99.62%	230	99.62%	230	99.62%
QD	BS	0	559	558	0.18%	558	0.18%	558	0.18%
		1	5031	558	88.91%	558	88.91%	558	88.91%
		2	45279	558	98.77%	558	98.77%	558	98.77%
		3	407511	558	99.86%	558	99.86%	558	99.86%
		4	3667599	558	99.98%	558	99.98%	558	99.98%
	S	0	559	558	0.18%	558	0.18%	558	0.18%
		1	3913	558	85.74%	558	85.74%	558	85.74%
		2	27391	558	97.96%	558	97.96%	558	97.96%
		3	191737	558	99.71%	558	99.71%	558	99.71%
		4	1342159	558	99.96%	558	99.96%	558	99.96%
	K	0	559	558	0.18%	558	0.18%	558	0.18%
		1	2236	558	75.04%	558	75.04%	558	75.04%
		2	8944	558	93.76%	558	93.76%	558	93.76%
		3	35776	558	98.44%	558	98.44%	558	98.44%
		4	143104	558	99.61%	558	99.61%	558	99.61%

Table 10: Savings on EC blocks for 2 qubit Grover’s Search Algorithm circuit[9]

Tech	QECC	Concat	Orig	Th = 0.001	% save	Th = 0.01	% save	Th = 0.1	% save
IT	BS	0	22	0	100%	0	100%	0	100%
		1	198	0	100%	0	100%	0	100%
		2	1782	9	99.5%	9	99.5%	9	99.5%
		3	16038	9	99.94%	9	99.94%	9	99.94%
		4	144342	14	99.99%	9	99.99%	0	100%
	S	0	29	0	100%	0	100%	0	100%
		1	203	0	100%	0	100%	0	100%
		2	1421	7	99.5%	7	99.5%	7	99.5%
		3	9947	7	99.93%	7	99.93%	7	99.93%
		4	69629	7	99.99%	7	99.99%	7	99.99%
	K	0	29	0	100%	0	100%	0	100%
		1	116	0	100%	0	100%	0	100%
		2	464	9	98.06%	9	98.06%	9	98.06%
		3	1856	9	99.51%	9	99.51%	9	99.51%
		4	7424	9	99.88%	9	99.88%	9	99.88%
SC	BS	0	29	0	100%	0	100%	0	100%
		1	261	7	97.32%	0	100%	0	100%
		2	2349	25	98.94%	16	99.32%	9	99.62%
		3	21141	25	99.88%	25	99.88%	24	99.89%
		4	190269	25	99.99%	25	99.99%	25	99.99%
	S	0	29	0	100%	0	100%	0	100%
		1	203	5	97.54%	0	100%	0	100%
		2	1421	16	98.87%	16	98.87%	16	98.87%
		3	9947	16	99.84%	16	99.84%	16	99.84%
		4	69629	16	99.99%	16	99.99%	16	99.99%
	K	0	29	0	100%	0	100%	0	100%
		1	116	4	96.55%	0	100%	0	100%
		2	464	18	96.12%	18	96.12%	10	97.84%
		3	1856	18	99.03%	18	99.03%	18	99.03%
		4	7424	18	99.78%	18	99.78%	18	99.78%
LP	BS	0	21	20	4.76%	20	4.76%	20	4.76%
		1	189	20	89.42%	20	89.42%	20	89.42%
		2	1701	20	98.82%	20	98.82%	20	98.82%
		3	15309	20	99.87%	20	99.87%	20	99.87%
		4	137781	20	99.98%	20	99.98%	20	99.98%
	S	0	21	20	4.76%	20	4.76%	20	4.76%
		1	147	20	86.39%	20	86.39%	20	86.39%
		2	1029	20	98.05%	20	98.05%	20	98.05%
		3	7203	20	99.72%	20	99.72%	20	99.72%
		4	50421	20	99.96%	20	99.96%	20	99.96%
	K	0	21	20	4.76%	20	4.76%	20	4.76%
		1	84	20	76.19%	20	76.19%	14	83.33%
		2	336	20	94.05%	20	94.05%	14	95.83%
		3	1344	20	98.51%	14	98.96%	14	98.96%
		4	5376	14	99.74%	14	99.74%	14	99.74%
NP	BS	0	22	21	4.55%	9	59.1%	0	100%
		1	198	18	90.9%	18	90.9%	18	90.9%
		2	1782	18	98.99%	18	98.99%	18	98.99%
		3	16038	18	99.89%	18	99.89%	18	99.89%
		4	144342	18	99.99%	18	99.99%	18	99.99%
	S	0	22	21	4.55%	9	59.1%	0	100%
		1	154	18	88.31%	14	90.9%	14	90.9%
		2	1078	14	98.7%	14	98.7%	14	98.7%
		3	7546	14	99.81%	14	99.81%	14	99.81%
		4	52822	14	99.97%	14	99.97%	14	99.97%
	K	0	22	21	4.55%	9	59.1%	0	100%
		1	88	14	84.09%	14	84.09%	7	92.04%
		2	352	14	96.02%	14	96.02%	14	96.02%
		3	1408	14	99%	14	99%	14	99%
		4	5632	14	99.75%	14	99.75%	14	99.75%
NA	BS	0	22	21	4.55%	10	54.54%	1	95.45%
		1	198	21	89.39%	20	89.9%	20	89.9%
		2	1782	20	98.88%	20	98.88%	20	98.88%
		3	16038	20	99.87%	20	99.87%	20	99.87%
		4	144342	20	99.98%	20	99.98%	20	99.98%
	S	0	22	21	4.55%	10	54.54%	1	95.45%
		1	154	21	86.36%	20	87%	14	90.9%
		2	1078	20	98.14%	14	98.7%	14	98.7%
		3	7546	14	99.81%	14	99.81%	14	99.81%
		4	52822	14	99.97%	14	99.97%	14	99.97%
	K	0	22	21	4.55%	10	54.54%	1	95.45%
		1	88	20	77.27%	14	84.09%	14	84.09%
		2	352	14	96.02%	14	96.02%	14	96.02%
		3	1408	14	99%	14	99%	14	99%
		4	5632	14	99.75%	14	99.75%	14	99.75%
QD	BS	0	34	33	2.94%	33	2.94%	33	2.94%
		1	306	33	89.21%	33	89.21%	33	89.21%
		2	2754	33	98.8%	33	98.8%	33	98.8%
		3	24786	33	99.87%	33	99.87%	33	99.87%
		4	223074	33	99.98%	33	99.98%	33	99.98%
	S	0	34	33	2.94%	33	2.94%	33	2.94%
		1	238	33	86.13%	33	86.13%	33	86.13%
		2	1666	33	98%	33	98%	33	98%
		3	11662	33	99.72%	33	99.72%	33	99.72%
		4	81634	33	99.96%	33	99.96%	33	99.96%
	K	0	34	33	2.94%	33	2.94%	33	2.94%
		1	136	33	75.73%	33	75.73%	33	75.73%
		2	544	33	93.93%	33	93.93%	33	93.93%
		3	2176	33	98.48%	33	98.48%	33	98.48%
		4	8704	33	99.62%	33	99.62%	33	99.62%

Table 11: Savings on EC blocks for 4 qubit Reversible Adder circuit

Tech	QECC	Concat	Orig	Th = 0.001	% save	Th = 0.01	% save	Th = 0.1	% save
IT	BS	0	134	0	100%	0	100%	0	100%
		1	1206	0	100%	0	100%	0	100%
		2	10854	72	99.34%	72	99.34%	72	99.34%
		3	97686	72	99.92%	72	99.92%	72	99.92%
		4	879174	76	99.99%	66	99.99%	4	99.999%
	S	0	134	0	100%	0	100%	0	100%
		1	938	0	100%	0	100%	0	100%
		2	6566	35	99.47%	35	99.47%	35	99.47%
		3	45962	35	99.92%	35	99.92%	35	99.92%
		4	321734	35	99.98%	35	99.98%	35	99.98%
	K	0	134	0	100%	0	100%	0	100%
		1	536	0	100%	0	100%	0	100%
		2	2144	72	96.64%	72	96.64%	72	96.64%
		3	8576	72	99.16%	72	99.16%	72	99.16%
		4	34304	72	99.79%	72	99.79%	72	99.79%
SC	BS	0	183	2	98.91%	0	100%	0	100%
		1	1647	58	96.48%	9	99.45%	0	100%
		2	14823	168	98.87%	110	99.26%	62	99.58%
		3	133407	168	99.87%	168	99.87%	165	99.88%
		4	1200663	168	99.98%	168	99.98%	168	99.98%
	S	0	183	2	98.91%	0	100%	0	100%
		1	1281	34	97.34%	4	99.69%	0	100%
		2	8967	118	98.68%	118	98.68%	118	98.68%
		3	62769	118	99.81%	118	99.81%	118	99.81%
		4	439383	118	99.97%	118	99.97%	118	99.97%
	K	0	183	2	98.91%	0	100%	0	100%
		1	732	32	95.63%	7	99%	0	100%
		2	2928	129	95.6%	129	95.6%	65	97.78%
		3	11712	129	98.9%	129	98.9%	129	98.9%
		4	46848	129	99.72%	129	99.72%	129	99.72%
LP	BS	0	105	104	0.95%	104	0.95%	104	0.95%
		1	945	104	89%	104	89%	104	89%
		2	8505	104	98.78%	104	98.78%	104	98.78%
		3	76545	104	99.86%	104	99.86%	104	99.86%
		4	688905	104	99.98%	104	99.98%	104	99.98%
	S	0	105	104	0.95%	104	0.95%	104	0.95%
		1	735	104	85.85%	104	85.85%	104	85.85%
		2	5145	104	97.98%	104	97.98%	104	97.98%
		3	36015	104	99.71%	104	99.71%	104	99.71%
		4	252105	104	99.96%	104	99.96%	104	99.96%
	K	0	105	104	0.95%	104	0.95%	104	0.95%
		1	420	104	75.24%	104	75.24%	100	76.2%
		2	1680	100	94.05%	100	94.05%	100	94.05%
		3	6720	100	98.51%	100	98.51%	100	98.51%
		4	26880	100	99.63%	100	99.63%	100	99.63%
NP	BS	0	105	104	0.95%	51	51.43%	13	87.62%
		1	945	100	89.42%	100	89.42%	100	89.42%
		2	8505	100	98.82%	100	98.82%	100	98.82%
		3	76545	100	99.87%	100	99.87%	100	99.87%
		4	688905	100	99.99%	100	99.99%	100	99.99%
	S	0	105	104	0.95%	52	50.47%	7	93.33%
		1	735	104	85.85%	97	86.8%	97	86.8%
		2	5145	97	98.11%	97	98.11%	97	98.11%
		3	36015	97	99.73%	97	99.73%	97	99.73%
		4	252105	97	99.96%	97	99.96%	97	99.96%
	K	0	105	104	0.95%	52	50.47%	7	93.33%
		1	420	100	76.19%	100	76.19%	55	86.9%
		2	1680	100	94.05%	100	94.05%	100	94.05%
		3	6720	100	98.52%	100	98.52%	100	98.52%
		4	26880	100	99.63%	100	99.63%	100	99.63%
NA	BS	0	128	127	0.78%	57	55.47%	19	85.15%
		1	1152	127	88.97%	127	88.97%	127	88.97%
		2	10368	127	98.77%	127	98.77%	127	98.77%
		3	93312	127	99.86%	127	99.86%	127	99.86%
		4	839808	127	99.98%	127	99.98%	127	99.98%
	S	0	128	127	0.78%	57	55.67%	19	85.15%
		1	896	127	85.83%	125	86.05%	90	89.95%
		2	6272	127	97.97%	90	98.56%	90	98.56%
		3	43904	90	99.79%	90	99.79%	90	99.79%
		4	307328	90	99.997%	90	99.997%	90	99.997%
	K	0	128	127	0.78%	57	55.47%	19	85.15%
		1	512	127	75.2%	108	78.9%	108	78.9%
		2	2048	108	94.73%	108	94.73%	108	94.73%
		3	8192	108	98.68%	108	98.68%	108	98.68%
		4	32768	108	99.67%	108	99.67%	108	99.67%
QD	BS	0	190	189	0.5%	189	0.5%	189	0.5%
		1	1710	189	88.95%	189	88.95%	189	88.95%
		2	15390	189	98.77%	189	98.77%	189	98.77%
		3	138510	189	99.86%	189	99.86%	189	99.86%
		4	1246590	189	99.98%	189	99.98%	189	99.98%
	S	0	190	189	0.5%	189	0.5%	189	0.5%
		1	1330	189	85.8%	189	85.8%	189	85.8%
		2	9310	189	97.97%	189	97.97%	189	97.97%
		3	65170	189	99.71%	189	99.71%	189	99.71%
		4	456190	189	99.96%	189	99.96%	189	99.96%
	K	0	190	189	0.5%	189	0.5%	189	0.5%
		1	760	189	75.13%	189	75.13%	189	75.13%
		2	3040	189	93.78%	189	93.78%	189	93.78%
		3	12160	189	98.45%	189	98.45%	189	98.45%
		4	48640	189	99.61%	189	99.61%	189	99.61%